Advanced Materials Research Vol. 856 (2014) pp 215-219
Online available since 2013/Dec/06 at www.scientific.net

doi:10.4028/www.scientific.net/AMR.856.215

Effect of Gate Dielectrics on the Performance of P-Type Cu_2O TFTs Processed at Room Temperature

H. A. Al-Jawhari,[1,a] and J. A. Caraveo-Frescas[2]

[1]Department of Physics, King Abdulaziz University, Jeddah 21589, Saudi Arabia

[2]Materials Science and Engineering, King Abdullah University of Science and Technology (KAUST), Thuwal 23955-6900, Saudi Arabia

[a] haljawhari@kau.edu.sa

Keywords: Cuprous oxide thin films, P-type TFTs, high-κ gate dielectric, $SrTiO_3$ films.

Abstract. Single-phase Cu_2O films with p-type semiconducting properties were successfully deposited by reactive DC magnetron sputtering at room temperature followed by post annealing process at 200°C. Subsequently, such films were used to fabricate bottom gate p-channel Cu_2O thin film transistors (TFTs). The effect of using high-κ $SrTiO_3$ (STO) as a gate dielectric on the Cu_2O TFT performance was investigated. The results were then compared to our baseline process which uses a 220 nm aluminum titanium oxide (ATO) dielectric deposited on a glass substrate coated with a 200 nm indium tin oxide (ITO) gate electrode. We found that with a 150 nm thick STO, the Cu_2O TFTs exhibited a p-type behavior with a field-effect mobility of 0.54 $cm^2.V^{-1}.s^{-1}$, an on/off ratio of around 44, threshold voltage equaling -0.62 V and a sub threshold swing of 1.64 V/dec. These values were obtained at a low operating voltage of -2V. The advantages of using STO as a gate dielectric relative to ATO are discussed.

Introduction

Cuprous oxide, Cu_2O, is one of the most promising materials to be applied as a p-channel material for transparent thin-film transistors (TFTs). It has a cubic crystal structure with a direct band gap of 2.17eV [1], and high holes mobility exceeding 100 $cm^2.V^{-1}.s^{-1}$[2]. Its unique native p-type property is attributed to the presence of Cu^+ vacancy, which introduces an acceptor level about 0.3 eV above its valance band [3, 4].

Even though many high quality p-type Cu_2O films have already been achieved, there are only a few reports on using them as TFTs [5-7]. Recently, Fortunato et al [8] reviewed a detailed progress regarding this topic. However, due to the low or mediated value of the used gate dielectric, all the above-mentioned TFTs are not beneficial to low-power consumption. The only reported Cu_2O TFT with high-κ gate dielectric, was the work of Zou et al [9] where they used high-κ HfON as a gate dielectric. Their top-gate Cu_2O (TFT) achieved a superior performance with a high on-off current ratio of 3×10^6 and a large saturation mobility of 4.3 $cm^2.V^{-1}.s^{-1}$ at low operating voltages (V_D=−3V, V_G = −3V). Nevertheless, their device was processed by PLD at high deposition temperature of 500°C.

In this work, we demonstrate the ability of using strontium titanate $SrTiO_3$ (STO) as a high-κ dielectric with Cu_2O thin films prepared at room temperature to fabricate low power p-type Cu_2O (TFTs). Strontium titanate $SrTiO_3$ (STO) is known as one of the best characterized perovskite class materials; it has a cubic crystal structure with the advantage of a high dielectric constant of ε_r = 300 for bulk material at room temperature. STO has been used as a gate dielectric for some organic TFTs [10, 11], or MOSFETs [12] but so far, it has not yet been used with Cu_2O TFTs.

Experimental Details

Prior to the TFTs fabrication, Copper oxide films were deposited on a 100-nm SiO_2/Si substrate by reactive DC magnetron sputtering at room temperature. The relative oxygen partial pressures (O_{pp}), deposition pressure, total gas flow (Ar+O_2), and the dc power were 10%, 4.5 mTorr, 40 sccm and

50 W, respectively. The microstructures of the deposited films were characterized by X-ray diffraction (XRD). Hall measurements were carried out using the van der Pauw configuration at room temperature to obtain hole mobility and concentration, while Seebeck measurements were executed between (300K- 450K) to confirm the films polarity. To fabricate Cu_2O TFTs, 150 nm $SrTiO_3$ was deposited by pulsed laser deposition (PLD) as a gate dielectric on top of a 25 nm Pt-coated SiO_2/Si substrate. The active layer consisting of 30 nm of Cu_2O was then deposited. Finally, the Pt film of 80nm was evaporated on Cu_2O surface by electron-beam evaporation, and source/drain electrodes were defined by our local shadow masks to achieve active channels with a W/L= 250µm/50µm. The whole device was then annealed at 200 ^oC in air for 3 hours. Cross section morphology of fabricated devices was characterized by Tunneling electron microscopy (TEM).The electrical transport properties of TFTs were measured by a Keithley 4200 precision semiconductor parameter analyzer. All electrical measurements were carried out under ambient atmospheric pressure at room temperature in the dark. The carrier field-effect mobility of the TFT was calculated in the linear regime, using the formula

$$\mu_{FE} = \frac{\partial I_D}{\partial V_D} \cdot \frac{L}{W C_{ox} V_D} \quad (1)$$

where C_{ox} is the capacitance of the gate dielectric. Threshold voltage (V_{Th}) were extracted from the (I_D-V_G) transfer characteristics, while subthreshold swing (SS), which is defined as $SS=[\partial V_G/\partial \log(I_D)]$, was evaluated using the slope of the weak-region of (log (I_D)-V_G) plot, where $V_G<V_T$. The maximum number of traps D_{it} at the oxide/dielectric interface was then estimated as

$$D_{it} = \left[\frac{SS.\log(e)}{KT/q} - 1\right]\frac{C_{ox}}{q} \quad (2)$$

Results and Discussion

Characterizations of Cu_2O Thin films. The XRD results and the relative orientation of the as-deposited film and that annealed for 3 hours are shown in Fig.1 (a). In both cases, the reflection peaks indicate a fully (111) preferred orientation Cu_2O structure without any trace of Cu or CuO phases. It is clear from the figure that the annealing process does not affect the structure of the films nor their orientation. However, the increase in intensity associated with the annealing process reveals the improvement in the crystallinity of the films.

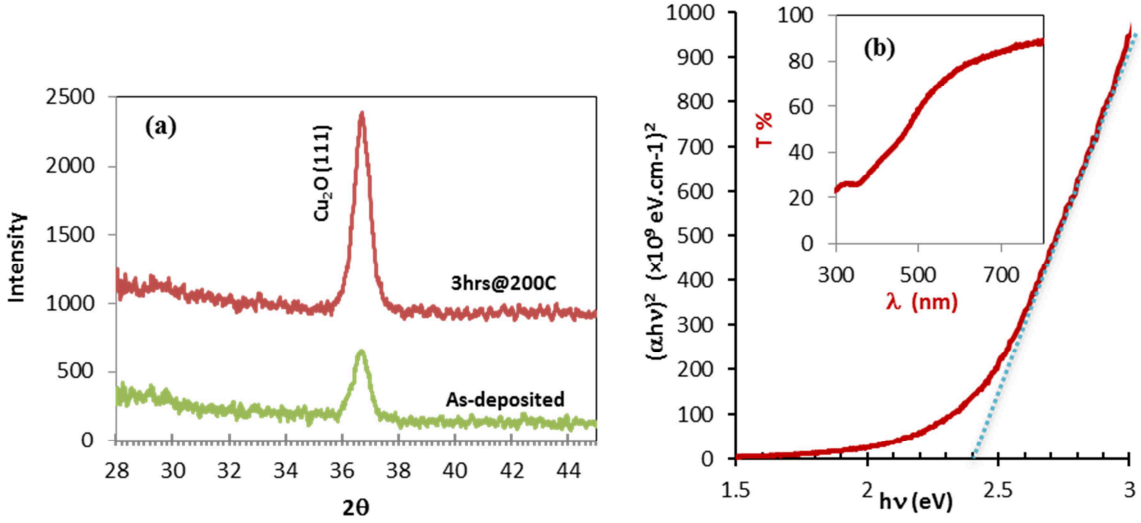

Fig.1. (a) XRD pattern of both the as-deposited Cu_2O film and that annealed at 200^oC for 3 hours. (b) The transmittance curve and extracted E_g for the annealed film.

Hall measurements obtained from films that annealed at 200^oC in air for 3 hours showed that the films had p-type semiconducting electrical properties with hole mobility and carrier concentration of 16 $cm^2.V^{-1}.s^{-1}$ and 10^{16} cm^{-3} respectively. The positive polarity of the Cu_2O film was confirmed

by thermoelectric measurements, where annealed films showed a Seebeck coefficient of 250 μVK^{-1} with temperatures ranging from 300K to 450K. The same films deposited on a glass substrate showed an average optical transmittance of 70.4% in the optical range (400-800nm), with an extracted energy gap of E_g=2.4eV as shown in Fig.1 (b).

Characterizations of Pt/STO/Pt stack. Measuring the I–V curve of the Pt/STO/Pt stack at room temperature, we found that the 150nm-STO layer could usually withstand voltages of about 2V which corresponds to a breakdown field of around 133 $kV.cm^{-1}$. The capacitance was generally measured with an LCR meter at a test frequency of 100 kHz. To further characterize the dielectric, the capacitance was also measured with frequencies ranging from 10kHz to 1MHz. Between 10-40 kHz the capacitance dropped sharply to 20% of its value. After that, and up to 500 kHz, the dielectric frequency response was almost constant. Using two different circular electrodes with radii of 250μm and 150 μm, the values obtained for κ were ~27 and 39 respectively. The average value of capacitance per unit area, C_{ox}, was then estimated to be about 200 $nF.cm^{-2}$.

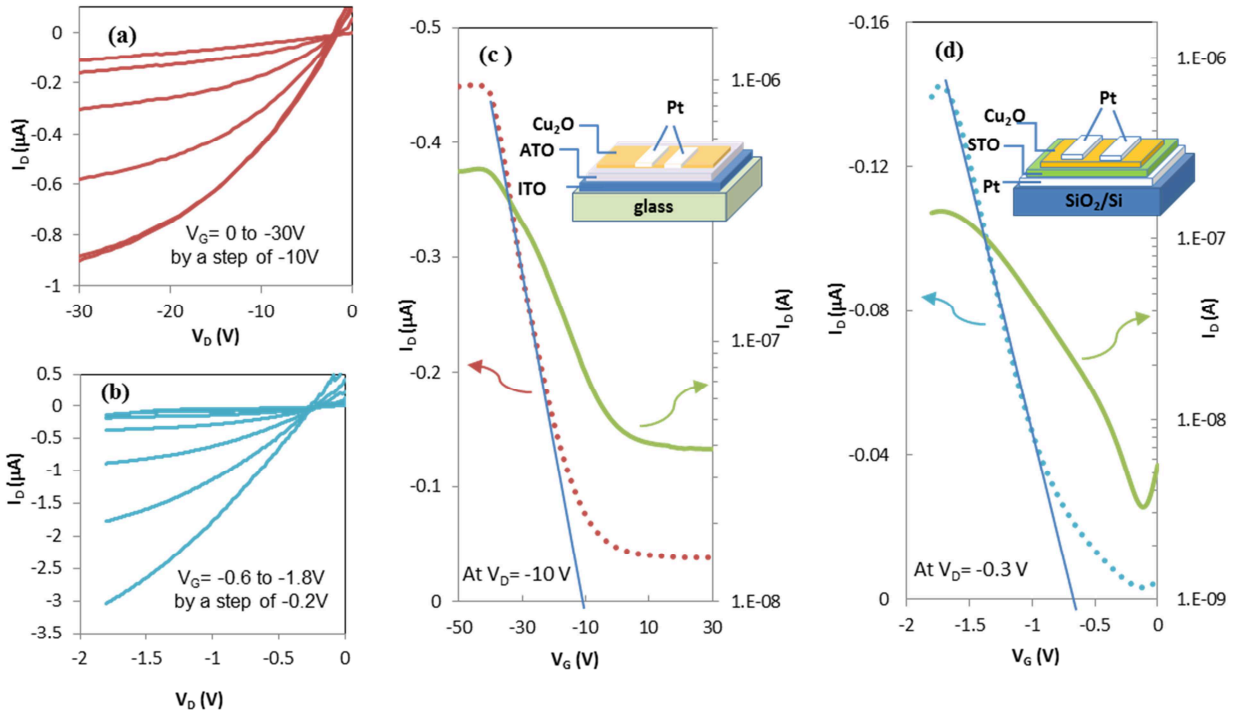

Fig.2. Output characteristics of our Cu_2O TFTs using (a) ATO and (b) STO as gate dielectrics. Corresponding transfer curves at (c) V_D=-10V for ATO device, and (d) V_D=-0.3V for STO device along with schematic diagram of TFT prototypes.

Characterizations of Cu_2O TFTs. In order to investigate the effect of the dielectric material on the device performance, we built our first set of Cu_2O TFTs according to our baseline process which uses 220 nm (ATO) dielectric deposited on a glass substrate coated with a 200 nm (ITO) gate electrode. Fig.2 (a) shows the output characteristics of a 30 nm Cu_2O TFT. The gate voltage V_G is varied from 0 to -50 V by a step of -10V, while the drain voltage is swept from 0 to -30V. The linear mobility and threshold voltage for the device were extracted at V_D =−10 V using the transfer curve shown in Fig.2 (c). The Cu_2O/ATO TFTs exhibited a p-type behavior with a linear mobility of $2.3x10^{-3}$ $cm^2.V^{-1}.s^{-1}$, an on/off ratio around 17 and a threshold voltage around −10V. These values are similar to those obtained by Fortunato et al. [8] using the same gate dielectric, however, their films were subjected to annealing treatment for 10 hours instead of 3. Replacing the ATO gate dielectric with the high-κ STO had a dramatic effect on the performance of our Cu_2O devices. Fig.2 (b) shows the output characteristics of the Cu_2O TFTs, using STO as a gate dielectric, where the drain voltage V_D is swept from 0 to −1.8 V and the gate voltage V_G is stepped between 0 and −1.8 V. We found that only low voltages were required to achieve a pronounced variation of the source-drain current. Saturation was hardly obtained since the dielectric breakdown occurred before the

drain current reached its maximum value. A noticeable positive leakage current at small V_D and high V_G was also observed; this current comes from leaks outside the active channel of the transistor and can be terminated by proper patterning of the gate electrode and/or the oxide channel. The corresponding transfer characteristics of Cu_2O TFT with STO at V_D =−0.3 V are presented in Fig.2 (d).

Table 1. Linear field-effect mobility (μ_{FE}), threshold voltage (V_{Th}), subthreshold swing (SS), and maximum number of interface traps (D_{it}) for the both TFTs after being annealed at 200°C in air.

Gate Dielectric	μ_{FE} ($cm^2.V^{-1}.s^{-1}$)	V_{Th} (V)	SS (V/dec)	D_{it} $\times 10^{13}$ (cm^{-2})
ATO	2.3×10^{-3}	-10.75	31.85	18.5
STO	1.642	-0.62	1.642	3.319

The most important parameters for the two different sets of Cu_2O TFTs are summarized in Table.1. Although the mobility was enhanced by two orders of magnitude, it is still smaller than what we expected to achieve using a high-κ insulator such as STO. One possible reason behind such relatively low mobility could be the local polarization effects that are usually associated with the high-κ insulator. It is well known that carrier localization is enhanced by insulators with large permittivities, due to the random dipole field present at the interface [13]. Another possible reason is the non-homogeneity of the Cu_2O film on the STO layer. It has been commonly observed by other workers [14-16] that the Cu_2O nanoparticles or thin films grown on STO are typified by spontaneous self-assembly of Cu_2O islands or clusters, which is believed to be governed by the (8.9%) lattice mismatch between Cu_2O and the STO lattice. The cross-sectional TEM image of our device, shown in Fig.3, supports this proposal. It is clear that the morphology of Cu_2O film is not homogenous along the whole interface; some areas are smooth, where we believe our working electrodes are located, and some are formed as clusters. As a result of all these mechanisms, the Cu_2O/STO interface would exhibit high density of traps that kill the carriers and hence lower channel mobility.

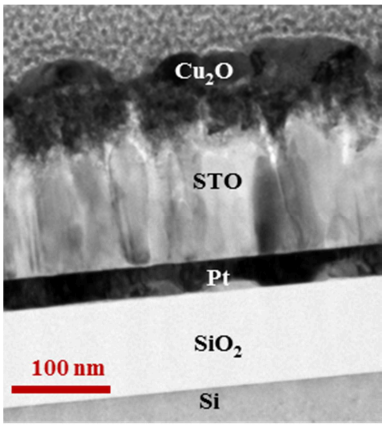

Fig.3. Cross-section TEM image of the Cu_2O/STO stack annealed at 200°C for 3hours.

We think introducing a buffer layer between Cu_2O and STO and/or adjusting the deposition power of Cu_2O films may help to create a smooth interface and, hence, a better device performance. However, to verify this, further investigations would be required.

Conclusion

The effect of the gate dielectric on the electrical characteristics of p-channel Cu_2O thin film transistors was investigated. We found that using $SrTiO_3$ as a high-κ dielectric enhances the TFTs performance. Compared to our previous TFTs with ATO, the channel mobility of TFTs with STO has been increased by two orders of magnitude while the operating voltage dropped from -30V to around -2V.

Acknowledgment

The authors would like to thank S. Kumar for the deposition of STO films.

References

[1] Ghijsen, J., et al., Electronic *structure of Cu2O and CuO.* Phys. Rev. B, 1988. **38**(16): p. 11322-11330.

[2] Li, B.S., K. Akimoto, and A. Shen, *Growth of Cu(2)O thin films with high hole mobility by introducing a low-temperature buffer layer.* Journal of Crystal Growth, 2009. **311**(4): p. 1102-1105.

[3] Brattain, W.H., *The Copper Oxide Rectifier.* Reviews of Modern Physics, 1951. **23**(3): p. 203-212.

[4] Arana-Chavez, D., et al., *Modeling the Transport and Reaction Mechanisms of Copper Oxide CVD.* Chemical Vapor Deposition, 2010. **16**(10-12): p. 336-346.

[5] Matsuzaki, K., et al., *Effects of post-annealing on (110) Cu2O epitaxial films and origin of low mobility in Cu2O thin-film transistor.* physica status solidi (a), 2009. **206**(9): p. 2192-2197.

[6] Fortunato, E., et al., *Thin-film transistors based on p-type Cu2O thin films produced at room temperature.* Appl. Phys. Lett., 2010. **96**(19): p. 192102.

[7] Yao, Z.Q., et al., *Room temperature fabrication of p-channel Cu2O thin-film transistors on flexible polyethylene terephthalate substrates.* Appl. Phys. Lett., 2012. **101**(4): p. 042114.

[8] Fortunato, E., P. Barquinha, and R. Martins, *Oxide semiconductor thin-film transistors: a review of recent advances.* Adv. Mater., 2012. **24**(22): p. 2945-86.

[9] Zou, X.A., et al., *Top-Gate Low-Threshold Voltage p-Cu2O Thin-Film Transistor Grown on SiO2/Si Substrate Using a High-kappa HfON Gate Dielectric.* Ieee Electron Device Letters, 2010. **31**(8): p. 827-829.

[10] Roth, F. and M. Huth, *High-κ field-effect transistor with copper-phthalocyanine.* Journal of Physics D: Applied Physics, 2011. **44**(37): p. 375102.

[11] Yan, H. and H. Okuzaki, *SrTiO3 insulator for low-voltage organic field-effect transistors.* Synthetic Metals, 2011. **161**(17-18): p. 1781-1786.

[12] Eisenbeiser, K., et al., *Field effect transistors with SrTiO[sub 3] gate dielectric on Si.* Applied Physics Letters, 2000. **76**(10): p. 1324.

[13] J. VERES, S.D.O., S. W. LEEMING, D. C. CUPERTINO and S. M. KHAFFAF, *Low k insulators as the choice of Dielectrics in Organic Field-Effect Transistors.* Adv. Funct. Mater. , 2003. **13**(3): p. 199.

[14] Yu, Z.Q., et al., *Epitaxial growth and microstructure of Cu2O nanoparticle/thin films on SrTiO3(100).* Nanotechnology, 2007. **18**(11): p. 115601.

[15] Pallecchi, I., et al., *Epitaxial copper oxide thin films deposited on cubic oxide substrates.* Journal of Physics D: Applied Physics, 2008. **41**(12): p. 125407.

[16] Kuchibhatla, S.V.N.T., et al., *Morphology, orientation relationship, and stability analysis of Cu2O nanoclusters on SrTiO3 (100).* Applied Physics Letters, 2009. **95**(5): p. 053111-053111-3.

Material Science and Engineering Technology II
10.4028/www.scientific.net/AMR.856

Effect of Gate Dielectrics on the Performance of P-Type Cu_2O TFTs Processed at Room Temperature
10.4028/www.scientific.net/AMR.856.215